Co-HLEX: Experimental Parallel Hierarchical Recursive Layout System

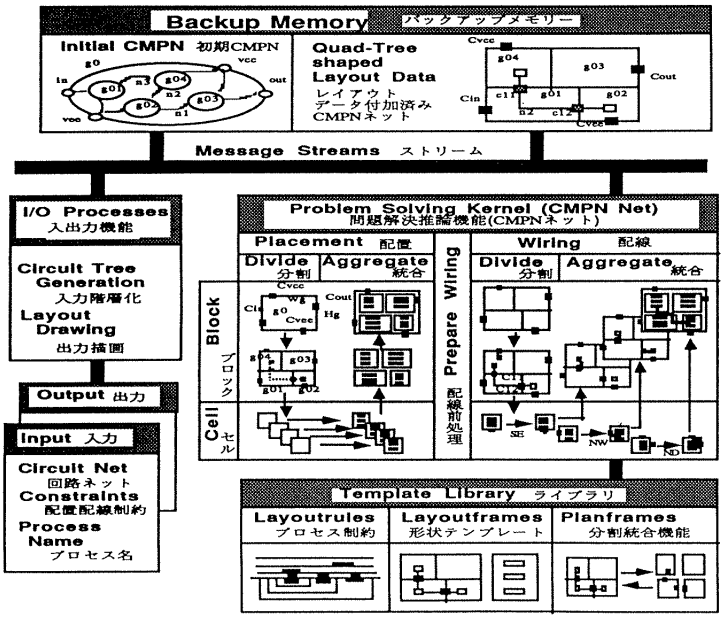
ABSTRACT

Experimental circuit layout system development to prove the effectiveness of FGCS paradigms.Generate a circuit layout diagram for a given circuit net and a planned chip shape.

KEY FEATURES

- Hierarchical Recursive Concurrent algorithm for placement and wiring.
- Streamed parallel computation paradigm for system description.
- Runtime co-operation to abut adjacent module layouts.
- New Parallel wiring algorithm composed of a patterned-global and a maze-local methods.
- Time complexity: nearly O(N) N = no.of modules in the circuit.
- Good speedup: nearly O(PE).

System Configuration

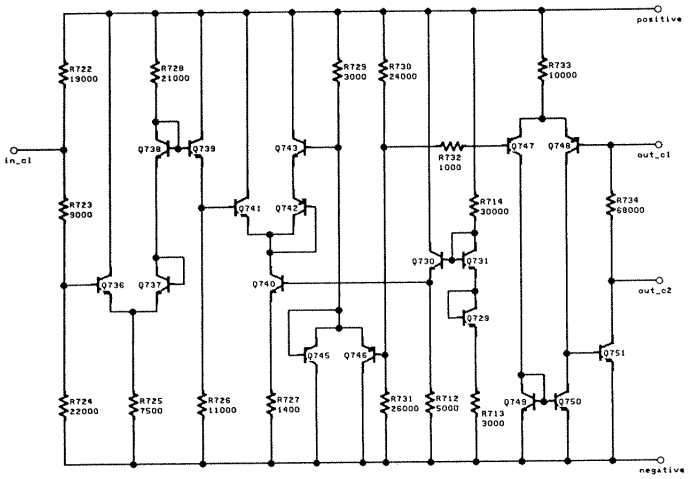


- Input: circuit net, planned layout shape,planned peripheralconnector placements.
- Processing:

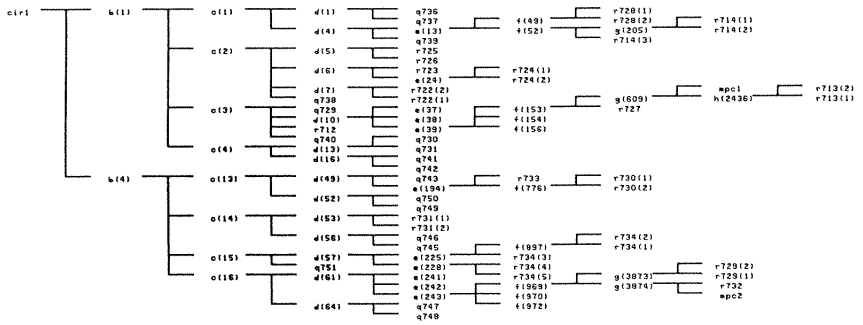
  Initial hierarchical CMPN (Circuit Module ProcessNetwork) generation from a given flat circuit net.

  Placement and wiring by using HRCTL algorithm.
- Output: Layout diagram display.

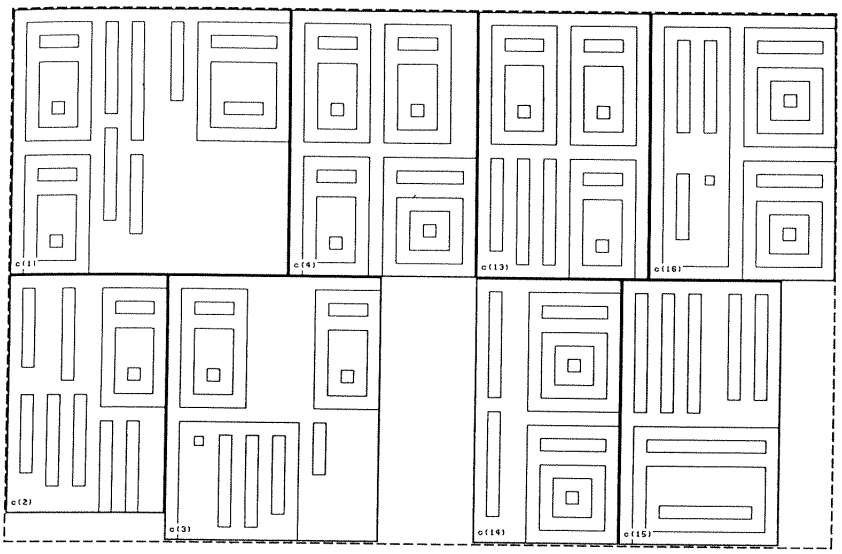
(1) Circuit network display and problem definition.

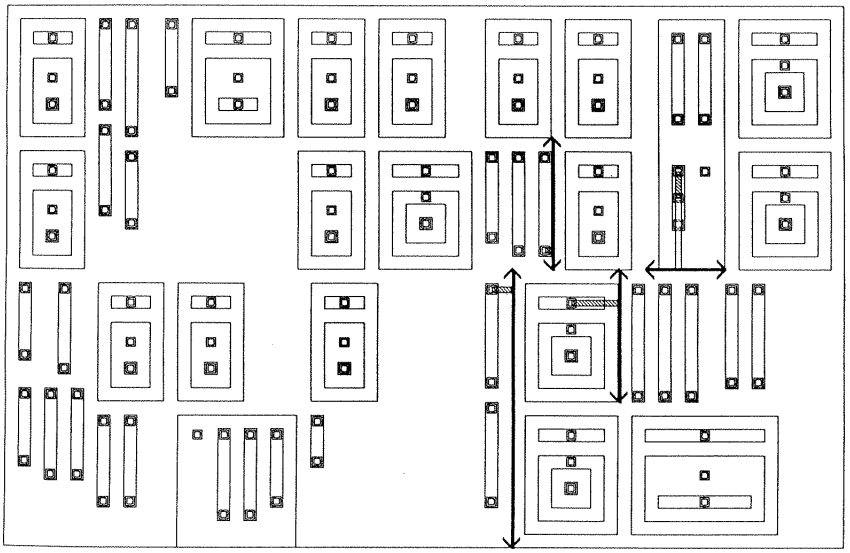


(2) Initial CMPN generation.

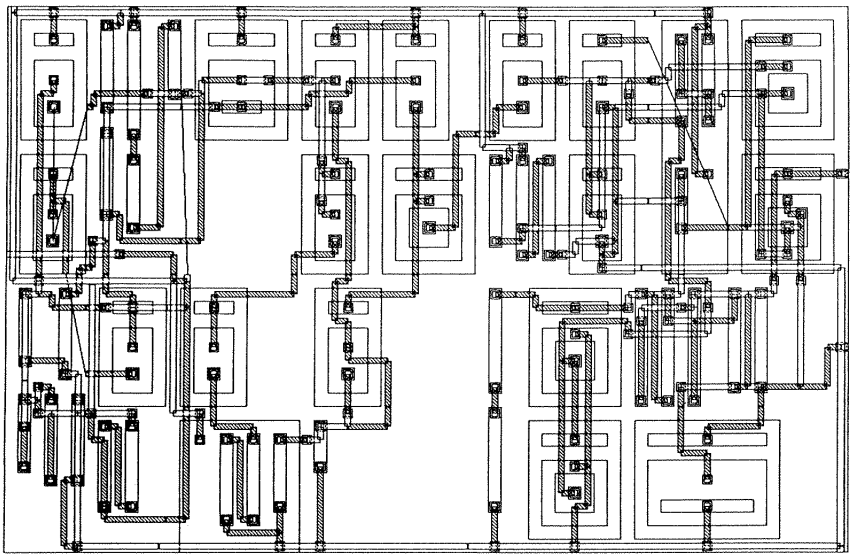


(3) HRCTL algorithm for placement and wiring.





(4) Final layout(46 moduled bipolar analog circuit).



(5) Layouts for a nearly 1000 moduled circuit and performance summary(explain by slides).