A Survey of Parallel Logic and Behavioral Simulation Techniques*

Professor Michael Lightner
Department of Electrical and Computer Engineering
University of Colorado
Boulder, CO USA
lightner@boulder.colorado.edu

Abstract

The huge size of digital circuits, many containing millions of transistors and over 100,000 logic gates would seem to provide great opportunity for the application of parallel computing techniques. Indeed, significant research has been directed toward the application of parallel computing in all aspects of VLSI CAD. In this talk we will examine the particular problem of simulating digital systems. We will concentrate on the logic and behavioral levels of abstraction.

The talk will begin with a brief overview of the techniques used for sequential simulation. We will then examine how the existing sequential techniques have been parallelized using different machine models. This will include strategies which partition circuits and those which also partition input patterns. We will also assess the success that these techniques have reported and where the bottlenecks have developed.

Many of the bottlenecks have been associated with the general purpose parallel machines that have been used by researchers. This leads use to the survey of special purpose simulation machines and their strategies, successes and failures.

At this point in the talk we will have exhausted general and specific parallel machine implementation of standard techniques for sequential simulation. This will lead to non-standard techniques for parallel simulation known as asynchronous techniques which include the ideas in Time-Warp and Chandy-Misra-Bryant. The asynchronous techniques will be discussed and the present state-of-the-art in this area will be assessed.

When the level of abstraction increases from the logic level to the behavioral level many techniques have to change. In fact, parallelizing high level models looks very much like parallelizing compiler techniques. Techniques in this area includes compiler and simulation based partitioning of hardware description languages combined with techniques from parallel logic simulation. Work in this area will be reviewed and future directions summarized.

We finish the survey with suggestions for future research and possibilities of new paradigms that will combine logic simulation with logic synthesis and logic verification, in both serial and parallel implementations, to provide effective design tools in the future.

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