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Overview of the Ten Years of the FGCS Project

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Abstract

This paper introduces how the FGCS Project started, its overall activities and the results of the FGCS project. The FGCS Project was launched in 1982 after a three year preliminary study stage. The basic framework of the fifth generation computer is parallel processing and inference processing based on logic programming. Fifth generation computers were viewed as suitable for the knowledge information processing needs of the near future. ICOT was established to promote the FGCS Project. This paper shows not only, ICOT's efforts in promoting the FGCS project, but relationship between ICOT and related organizations as well. I, also, conjecture on the parallel inference machines of the near future.

1 Preliminary Study Stage for the FGCS Project

The circumstances prevailing during the preliminary stage of the FGCS Project, from 1979 to 1981, can be summarized as follows.

·Japanese computer technologies had reached the level of the most up-to-date overseas computer technologies.

·A change of the role of the Japanese national project for computer technologies was being discussed whereby there would be a move away from improvement of industrial competitiveness by catching up with the latest European computer technologies and toward world-wide scientific contribution through the risky development of leading computer technologies.

In this situation, the Japanese Ministry of International Trade and Industry (MITI) started study on a new project - the Fifth Generation Computer Project. This term expressed MITI's will to develop leading technologies that would progress beyond the fourth generation computers due to appear in the near future and which would anticipate upcoming trends.

The Fifth Generation Computer Research Committee and its subcommittee (Figure 1-1) were established in 1979. It took until the end of 1981 to decide on target technologies and a framework for the project.

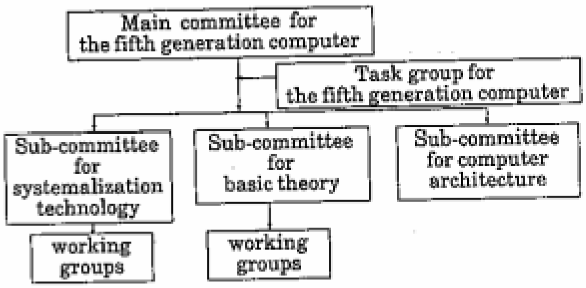

Figure 1-1 Organization of the Fifth Generation Computer Committee

Well over one hundred meetings were held with a similar number of committee members participating. The following important near-future computer technologies were discussed.

- Inference computer technologies for knowledge processing
- Computer technologies to process large-scale data bases and knowledge bases
- High performance workstation technologies
- Distributed functional computer technologies
- Super-computer technologies for scientific calculation

These computer technologies were investigated and discussed from the standpoints of international contribution by developing original Japanese technologies, the important technologies in future, social needs and conformance with Japanese governmental policy for the national project.

Through these studies and discussions, the committee decided on the objectives of the project by the end of 1980, and continued future studies of technical matters, social impact, and project schemes.

The committee's proposals for the FGCS Project are summarized as follows.

① The concept of the Fifth Generation Computer: To have parallel (non-Von Neumann) processing and inference processing using knowledge bases as basic mechanisms. In order to have these mechanisms, the hardware and software interface is to be a logic program language (Figure 1-2).

② The objectives of the FGCS project: To develop these innovative computers, capable of knowledge information processing and to overcome the technical restrictions of conventional computers.

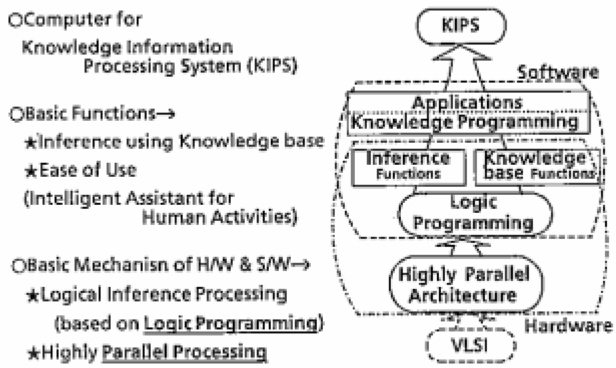

Figure 1-2 Concept of the Fifth Generation Computer

③ The goals of the FGCS project: To research and develop a set of hardware and software technologies for FGCS, and to develop an FGCS prototype system consisting of a thousand element processors with inference execution speeds of between 100M LIPS and 1G LIPS (Logical Inferences Per Second).

④ R&D period for the project: Estimated to be 10 years, divided into three stages.

- 3-year initial stage for R&D of basic technologies
- 4-year intermediate stage for R&D of sub-systems
- 3-year final stage for R&D of total prototype system

MITI decided to launch the Fifth Generation Computer System (FGCS) project as a national project for new information processing, and made efforts to acquire a budget for the project.

At the same time, the international conference on FGCS '81 was prepared and held in October 1981 to announce these results and to hold discussions on the topic with foreign researchers.

2 Overview of R&D Activities and Results of the FGCS Project

2.1 Stages and Budgeting in the FGCS Project

The FGCS project was designed to investigate a large number of unknown technologies that were yet to be developed. Since this involved a number of risky goals, the project was scheduled over a relatively long period of ten years. This ten-year period was divided into three stages.

- In the initial stage (fiscal 1982-1984), the purpose of R&D was to develop the basic computer technologies needed to achieve the goal.
- In the intermediate stage (fiscal 1985-1988), the purpose of R&D was to develop small to medium subsystems.
- In the final stage (fiscal 1989-1992), the purpose of R&D was to develop a total prototype system. The final stage was initially planned to be three years. After reexamination halfway through the final stage, this stage was extended to four years to allow evaluation and improvement of the total system in fiscal year 1992. Consequently, the total length of this project has been extended to 11 years.

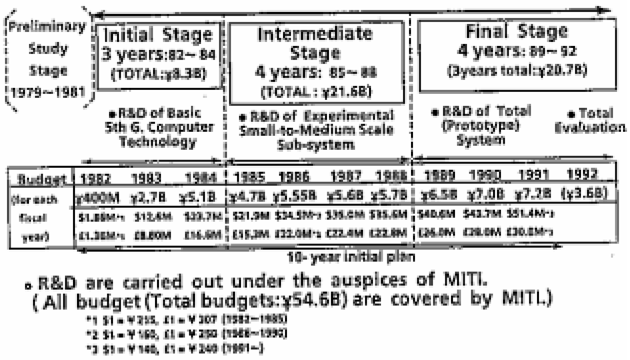

Figure 2-1 Budgets for the FGCS project

Each year the budget for the following years R&D activities was decided. MITI made great efforts in negotiating each year's budget with the Ministry of Finance. The budgets for each year, which are all covered by MITI, are shown in Figure 2-1. The total budget for the 3-year initial stage was about 8 billion yen. For the 4-year intermediate stage, it was about 22 billion yen. The total budget for 1989 to 1991 was around 21 billion yen. The budget for 1992 is estimated to be 3.6 billion yen.

Consequently, the total budget for the 11-year period of the project will be about 54 billion yen.

2.2 R&D subjects of each stage

At the beginning, it was considered that a detailed R&D plan could not be decided in detail for a period as long as ten years. The R&D goals and the means to reach these goals were not decided in detail. During the project, goals were sought and methods decided by referring back to the initial plan at the beginning of each stage.

The R&D subjects for each stage, shown in Figure 2-2, were decided by considering the framework and conditions mentioned below.

We defined 3 groups of 9 R&D subjects at the beginning of the initial stage by analyzing and rearranging the 5 groups of 10 R&D subjects proposed by the Fifth Generation Computer Committee.

At the end of the initial stage, the basic research themes of machine translation and speech, figure and image processing were excluded from this project. These were excluded because computer vender efforts on these technologies were recognized as having become very active.

In the middle of the intermediate stage, the task of developing a large scale electronic dictionary was transferred to EDR (Electronic Dictionary Research Center), and development of CESP (Common ESP system on UNIX) was started by AIR (AI language Research Center).

The basic R&D framework for promoting this project is to have common utilization of developed software by unifying the software development environment (especially by unifying programming languages). By utilizing software development systems and tools, the results of R&D can be evaluated and improved. Of course, considering the nature of this project, there is another reason making it difficult or impossible to use commercial products as a software development environment.

In each stage, the languages and the software development environment are unified as follows .

- Initial stage: Prolog on DEC machine
- Intermediate stage: ESP on PSI and SIMPOS
- Final stage: KL1 on Multi-PSI (or PIM) and PIMOS (PSI machines are also used as pseudo multi-PSI systems.) (Figure 2-6)

2.3 Overview of R&D Results of Hardware System

Hardware system R&D was carried out by the subjects listed listed below in each stage.

① Initial stage

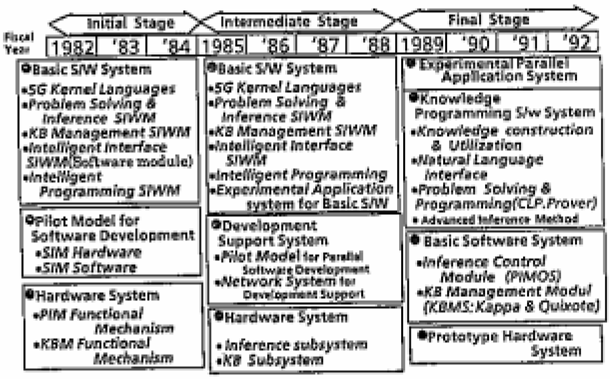

Figure 2-2 Transition of R&D subjects in each stage

ⓐ Functional mechanism modules and simulators for PIM (Parallel Inference Machine) of the hardware system

ⓑ Functional mechanism modules and simulators for KBM (Knowledge Base Machine) of the hardware system

ⓒ SIM (Sequential Inference Machine) hardware of pilot model for software development

② Intermediate Stage

ⓐ Inference subsystem of the hardware system .

ⓑ Knowledge base subsystem of the hardware system

ⓒ Pilot model for parallel software development of the development support system.

③ Final Stage

ⓐ Prototype hardware system

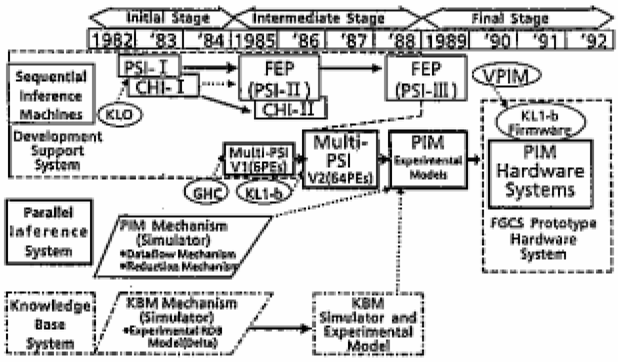

Figure 2-3 Transition of R&D results of Hardware System

The major R&D results on SIM were the PSI (Personal Sequential Inference Machine) and CHI (high performance back-end inference unit). In the initial stage, PSI- I (① ⓒ) was developed as KL0 (Kernel Language Version 0) machine. PSI- I had around 35 KLIPS (Logical Inference Per Second) execution speed. Around 100 PSI-Ⅰ machines were used as main WSs (workstations) for the sequential logic programming language, ESP, in the first half of the intermediate stage. CHI-Ⅰ (① ⓒ) showed around 200 KLIPS execution speed by using WAM instruction set and high-speed devices. In the intermediate stage, PSI was redesigned as multi-PSI FEP (Front End Processor) and PSI-Ⅱ, and has performance of around 330-400 KLIPS. CHI was also redesigned as CHI-Ⅱ (② ⓒ), with more than 400 KLIPS performance. PSI-Ⅱ machines were the main WSs for ESP after the middle of the intermediate stage, and were able to be used for KL1 by the last year of the intermediate stage. PSI-Ⅲ was developed as a commercial product by a computer company by using PIM/m CPU technologies, with the permission of MITI, and by using UNIX.

R&D on PIM continued throughout the project, as follows.

- In the initial stage, experimental PIM hardware simulators and software simulators with 8 to 16 processors were trial-fabricated based on data flow and reduction mechanisms (③ⓐ).
- In the intermediate stage, we developed multi-PSI V1, which was to construct 6 PSI-Is, as the first version of the KL1 machine. The performance of this machine was only several KLIPS because of the KL1 emulator (② ⓒ). It did, however, provide evaluation and experience by developing a very small parallel OS in KL1. This meant that we could develop multi-PSI V2 with 64 PSI-Ⅱ CPUs connected by a mesh network (② ⓐ). The performance of each CPU for KL1 was around 150 KLIPS, and the average performance of the full multi-PSI V2 was 5 MLIPS. This speed was enough to significantly improved to encourage efforts to develop various parallel KL1 software programs including an practical OS.
- After development of multi-PSI V2, we promote the design (② ⓐ) and trial-fabrication of PIM experimental models (③ⓐ).
- At present, we are completing development of prototype hardware consisting of 3 large scale PIM modules and 2 small scale experimental PIM modules (③ ⓐ). These PIM modules are designed to be equally suited to the KL1 machine for inference and knowledge base management, and to be able to be installed all programs written by KL1. This is in spite of their using different architecture.

The VPIM system is a KL1-b language processing system which gives a common base for PIM firmware for KL1-b developed on conventional computers.

R&D on KBM continued until the end of the intermediate stage. An experimental relational data base machine (Delta) with 4 relational algebraic engines was trial-fabricated in the initial stage (① ⓑ). During the intermediate stage, a deductive data base simulator was developed to use PSIs with an accelerator for comparison and searching. An experimental system was also developed with multiple-multiple name spaces, by using CHI. Lastly, a knowledge base hardware simulator with unification engines and multi-port page memory was developed in this stage (② ⓑ). We developed DB/KB management software, called Kappa, on concurrent basic software themes. At the beginning of the final stage, we thought that adaptability of PIM with Kappa for the various description forms for the knowledge base was more important than effectivity of KBM with special mechanism for the specific KB forms. In other words, we thought that deductive object-oriented DB technologies was not yet matured to design KBM as a part of the prototype system.

2.4 Overview of R&D Results of Software Systems

The R&D of software systems was carried out by a number of subjects listed below in each stage.

① Initial stage

Basic software

- ⓐ 5G Kernel Languages
- ⓑ Problem solving and inference software module
- ⓒ Knowledge base management software module
- ⓓ Intelligent interface software module
- ⓔ Intelligent programming software module
- ⓕ SIM software of pilot model for development support

② Basic software system in the intermediate stage

- ⓐ-ⓔ (as in the initial stage)
- ⓕ Experimental application system for basic software module

③ Final stage

- Basic software system
  - ⓐ Inference Control module
  - ⓑ KB management module
- Knowledge programming software
  - ⓒ Problem solving and programming module
  - ⓓ Natural language interface module
  - ⓔ Knowledge construction and utilization module
  - ⓕ Advanced problem solving inference method

ⓔ Experimental parallel application system

To make the R&D results easy to understand, I will separate the results for languages, basic software, knowledge programming and application software.

2.4.1 R&D results of Fifth Generation Computer languages

As the first step in 5G language development, we designed sequential logic programming languages KL0 and ESP (Extended Self-contained Prolog) and developed these language processors (① ⓐ). KL0, designed for the PSI hardware system, is based on Prolog. ESP has extended modular programming functions to KL0 and is designed to describe large scale software such as SIMPOS and application systems.

As a result of research on parallel logic programming language, Guarded Horn Clauses, or GHC, was proposed as the basic specification for KL1 (Kernel Language Version 1) (①ⓐ). KL1 was, then, designed by adding various functions to KL1 such as a macro description (②ⓐ). KL1 consists of a machine level language (KL1-b (base)), a core language (KL1-c) for writing parallel software and pragma (KL1-p) to describe the division of parallel processes. Parallel inference machines, multi-PSI and PIM, are based on KL1-b. Various parallel software, including PIMOS, is written in KL1-c and KL1-p.

A'um is an object oriented language. The results of developing the A'um experimental language processor reflect improvements in KL1 (②ⓐ, ③ⓐ).

To research higher level languages, several languages were developed to aid description of specific research fields. CIL (Complex Indeterminate Language) is the extended language of Prolog that describes meanings and situations for natural language processing (① ⓓ, ② ⓓ). CRL (Complex Record Language) was developed as a knowledge representation language to be used internally for deductive databases on nested relational DB software (② ⓒ). CAL (Contrainte Avec Logique) is a sequential constraint logic language for constraint programming (②ⓑ).

Mandala was proposed as a knowledge representation language for parallel processing, but was not adopted because it lacks a parallel processing environment and we had enough experience with it in the initial stage (①ⓒ).

Quixote is designed as a knowledge representation language and knowledge-base language for parallel processing based on the results of evaluation by CIL and CRL. Quixote is also a deductive object-oriented database language and play the key role in KBMS. A language processor is currently being developed for Quixote.

GDCC(Guarded Definite Clause with Constraints)

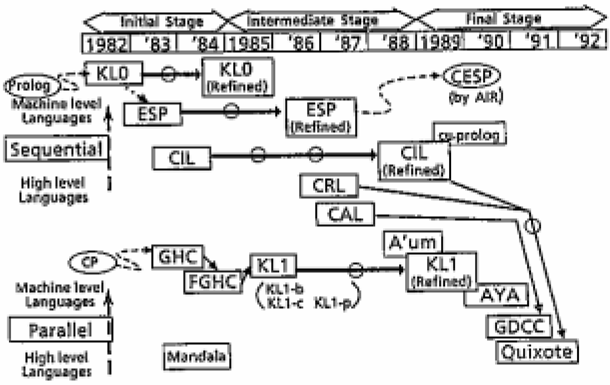

Figure 2-4 Transition of R&D of 5G Languages

is a parallel constraint logic language that processes CAL results.

2.4.2 R&D Results of Basic Software (OS)

In the initial stage, we developed a preliminary programming and operating system for PSI, called SIMPOS, using ESP (① ⓔ ⓕ). We continued to improve SIMPOS by adding functions corresponding to evaluation results. We also took into account the opinions of inside users who had developed software for the PSI machine using SIMPOS (②ⓑⓕ).

Since no precedent parallel OS which is suited for our aims had been developed anywhere in the world, we started to study parallel OS using our experiences of SIMPOS development in the initial stage. A small experimental PIMOS was developed on the multi-PSI V1 system in the first half of the intermediate stage (② ⓑ). Then, the first version of PIMOS was developed on the multi-PSI V2 system, and was used by KL1 users (② ⓑ). PIMOS continued to be improved by the addition of functions such as remote access, file access and debugging support (③ⓐ).

The Program Development Support System was also developed by the end of the intermediate stage (②ⓑ).

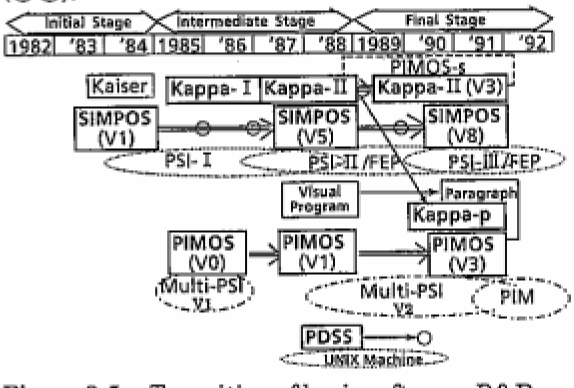

Figure 2-5 Transition of basic software R&D

Paragraph was developed as a parallel programming support system for improving concurrency and load distribution by the indication results of parallel processing (③ⓐ).

In regard to DB/KB management software, Kaiser was developed as a experimental relational DB management software in the initial stage (① ⓒ). Then, Kappa-Ⅰ and Kappa-Ⅱ were developed to provide the construction functions required to build a large scale DB/KB that could be used for natural language processing, theorem proving and various expert systems (② ⓒ). Kappa-Ⅰ and Kappa-Ⅱ ,based on nested relational model, are aimed at the database engine of deductive object-oriented DBMS .

Recently, a parallel version of Kappa , Kappa-P, is being developed. Kappa-P can manage distributed data bases stored on distributed disks in PIM. (③ ⓑ) Kappa-P and Quixote constitute the KBMS.

2.4.3 R&D Results of Problem Solving and Programming Technologies

Throughout this project, from the viewpoint of similarity mathematical theorem proving and program specification, we have been investigating proving technologies. The CAP (Computer Aided Proof) system was experimentally developed in the initial stage (② ⓔ). TRS (Term Rewriting System) and Metis were also developed to support specific mathematical reasoning, that is, the inference associated equals sign (②ⓔ).

An experimental program for program verification and composition, Argus, was developed by the end of the intermediate stage (① ⓔ and ② ⓔ). These research themes concentrated on R&D into the MGTP theorem prover in the final stage(③ⓒ).

Meta-programming technologies, partial evaluation technologies and the learning mechanism were investigated as basic research on advanced problem solving and the inference method (①ⓑ, ②ⓑ, ③ⓕ).

2.4.4 R&D Results on Natural Language Processing Technologies

Natural language processing tools such as BUP (Bottom-Up Parser) and a miniature electronic dictionary were experimentally developed in the initial stage (① ⓓ). These tools were extended, improved and arranged into LTB (Language Tool Box). LTB is a library of Japanese processing software modules such as LAX (Lexical Analyzer), SAX (Syntactic Analyzer), a text generator and language data bases (②ⓓ, ③ⓓ).

An experimental discourse understanding system, DUALS, was implemented to investigate context processing and semantic analysis using these language processing tools (① ⓓ,② ⓓ). An experimental argument system, called Dulcinia, is being implemented in the final stage (③ⓓ).

2.4.5 R&D Results on Knowledge Utilization Technologies and Experimental Application Systems

In the intermediate stage we implemented experimental knowledge utilization tools such as APRICOT, based on hypothetical reasoning technology, and Qupras, based on qualitative reasoning technology (② ⓒ). At present, we are investigating such inference mechanisms for expert systems as assumption based reasoning and case based reasoning, and implementing these as knowledge utilization tools to be applied to the experimental application system (③ⓔ).

As an application system, we developed, in Prolog, an experimental CAD system for logic circuit design support and wiring support in the initial stage. We also developed several experimental expert systems such as a CAD system for layout and logic circuit design, a troubleshooting system, a plant control system and a go-playing system written in ESP (②ⓕ, etc.).

Small to medium parallel programs written in KL1 were also developed to test and evaluate parallel systems by the end of the intermediate stage. These were improved for application to PIM in the final stage. These programs are PAX (a parallel semantics analyzer), Pentomino solver, shortest path solver and Tsume-go.

We developed several experimental parallel systems, implemented using KL1 in the final stage, such as LSI-CAD system (for logical simulation, wire routing, block layout, logical circuit design), genetic information processing system, legal inference system based on case based reasoning, expert systems for troubleshooting, plant control and go-playing (3g).

Some of these experimental systems were developed from other earlier sequential systems in the intermediate stage while others are new application fields that started in the final stage.

2.5 Infrastructure of the FGCS Project

As explained in 2.2, the main language used for software implementation in the initial stage was Prolog. In the intermediate stage, ESP was mainly used, and in the final stage KL1 was the principle language.

Therefore, we used a Prolog processing system on a conventional computer and terminals in the initial stage. SIMPOS on PSI (Ⅰ and Ⅱ) was used as the workbench for sequential programming in

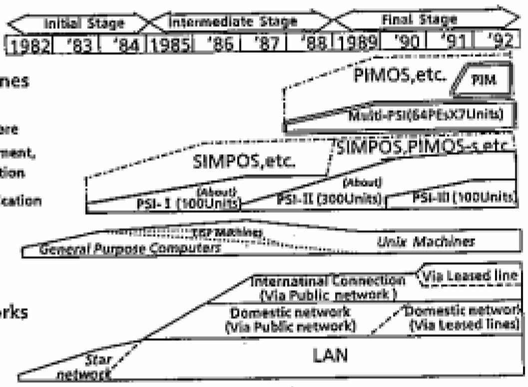

Figure 2-6 Infrastructure for R&D

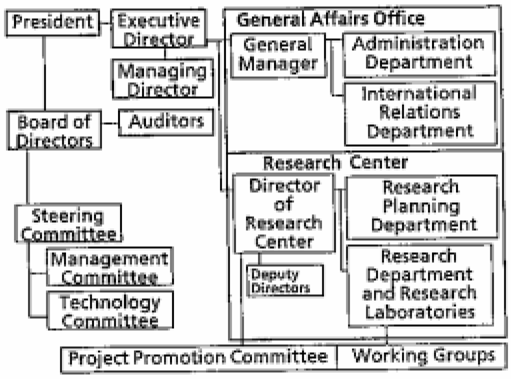

Figure 3-1 ICOT Organization

the intermediate stage. We are using PSI (Ⅱ and Ⅲ) as a workbench and remote terminals to parallel machines (multi-PSIs and PIMs) for parallel programming in the final stage. We have also used conventional machines for simulation to design PIM and a communication (E-mail, etc.) system.

In regard to the computer network system, LAN has been used as the in-house system, and LAN has been connected to domestic and international networks via gateway systems.

3 Promoting Organization of the FGCS Project

ICOT was established in 1982 as a non-profit core organization for promoting this project and it began R&D work on fifth generation computers in June 1982, under the auspices of MITI.

Establishment of ICOT was decided by considering the following necessity and effectiveness of a centralized core research center for promoting originative R&D,

- R&D themes should be directed and selected by powerful leadership, in consideration of hardware and software integration, based on a unified framework of fifth generation computers, throughout the ten-year project period.
- It was necessary to develop and nurture researchers working together because of the lack of researchers in this research field.
- A core center was needed to exchange information and to collaborate with other organizations and outside researchers.

ICOT consists of a general affairs office and a research center (Figure 3-1).

The organization of the ICOT research center was changed flexibly depending on the progress being made. In the initial stage, the research center consisted of a research planning department and three research laboratories. The number of laboratories was increased to five at the beginning of the intermediate stage. These laboratories became one research department and seven laboratories in 1990.

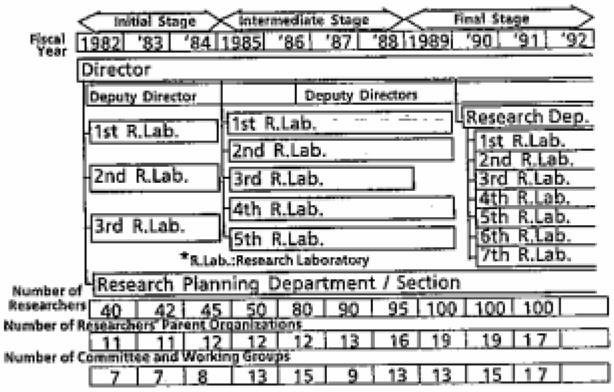

Figure 3-2 Transition of ICOT research center organization

The number of researchers at the ICOT research center has increased yearly, from 40 in 1982 to 100 at the end of the intermediate stage.

All researchers at the ICOT research center have been transferred from national research centers, public organizations, and computer vendors, and the like. To encourage young creative researchers and promote originative R&D, the age of dispatched researchers is limited to 35 years old. Because all researchers are normally dispatched to the ICOT research center for three to four years, ICOT had to receive and nurture newly transferred researchers. We must make considerable effort to continue to consistently lead R&D in the fifth generation computer field despite researcher rotation. This rotation has meant that we were able to maintain a staff of researchers in their 30's, and also could easily change the structure of organization in the ICOT research center.

In total, 184 researchers have been transferred to the ICOT research center with an average transfer period of 3 years and eight months (including around half of the dispatched researchers who are presently at ICOT).

The number of organizations which dispatched researchers to ICOT also increased, from 11 to 19. This increase in participating organizations was caused by an expanding scheme of the supporting companies, around 30 companies, to dispatch researchers to ICOT midway through the intermediate stage.

The themes each laboratory was responsible for changed occasionally depending on the progress being made.

Figure 3-3 shows the present assignment of research themes to each research laboratory.

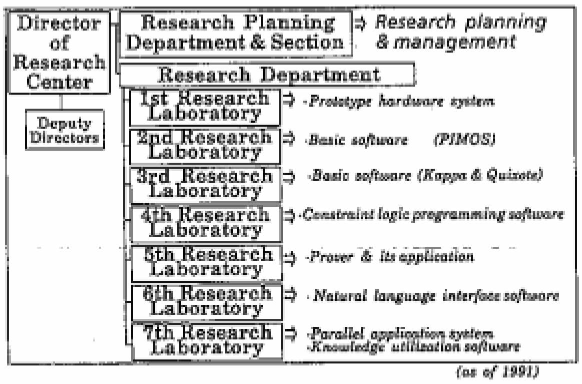

Figure 3-3 ICOT research center organization

Every year we invited several visiting researchers from abroad for several weeks at ICOT's expense to discuss and to exchange opinion on specific research themes with ICOT researchers. Up to the present, we have invited 74 researchers from 12 countries in this program.

We also received six long-term (about one year each) visiting researchers from foreign governmental organizations based on memorandums with the National Science Foundation (NSF) in the United States, the Institute National de Recherche en Informatique et Automatiqeu (INRIA) in France, and the Department of Trade and Industry (DTI) in the United Kingdom (Figures 3-2 and 3-4).

Figure 3-4 shows the overall structure for promoting this project. The entire cost for the R&D activities of this project is supported by MITI based on the entrust contract between MITI and ICOT. Yearly and at the beginning of each stage we negotiate our R&D plan with MITI. MITI receives advice of this R&D plan and evaluations of R&D results and ICOT research activities from the FGCS project advisory committee.

ICOT executes the core part of R&D and has contracts with eight computer companies for

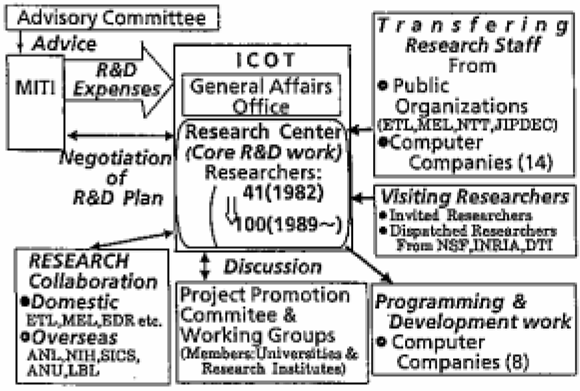

Figure 3-4 Structure for promoting FGCS project

experimental production of hardware and developmental software. Consequently, ICOT can handle all R&D activities, including the developmental work of computer companies towards the goals of this project.

ICOT has set up committee and working groups to discuss and to exchange opinions on overall plans results and specific research themes with researchers and research leaders from universities and other research institutes. Of course, construction and the themes of working groups are changed depending on research progress. The number of people in a working group is around 10 to 20 members, so the total number in the committee and working groups is about 150 to 250 each year.

Another program for information exchange and collaborative research activities and diffusion of research results will be described in the following chapter.

4 Distribution of R&D Results and International Exchange Activities

Because this project is a national project in which world-wide scientific contribution is very important, we have made every effort to include our R&D ideas, processes and project results when presenting ICOT activities. We, also, collaborate with outside researchers and other research organizations.

We believe these efforts have contributed to progress in parallel and knowledge processing computer technologies. I feel that the R&D efforts in these fields have increased because of the stimulative effect of this project. We hope that R&D efforts will continue to increase through distribution of this projects R&D results. I believe that many outside researchers have also made significant contributions to this project through their discussions and information exchanges with ICOT researchers.

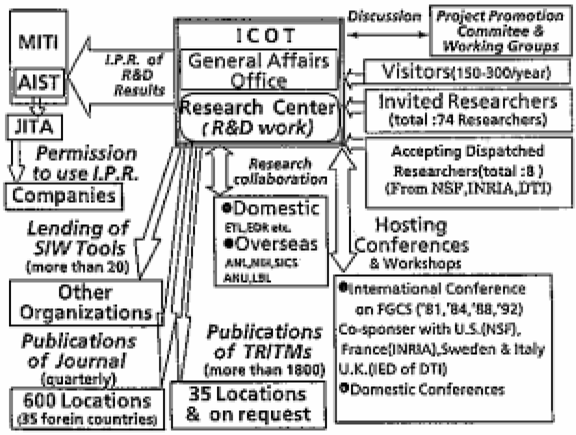

Figure 4-1 R&D result distribution and research collaboration

We could, for example, produce GHC, a core language of the parallel system, by discussion with researchers working on Parlog and Concurrent Prolog. We could, also, improve the performance of the PSI system by introducing the WAM instruction set proposed by Professor Warren.

We have several programs for distributing the R&D results of this project, to exchange information and to collaborate with researchers and organizations.

① One important way to present R&D activities and results is publication and distribution of ICOT journals and technical papers. We have published and distributed quarterly journals, which contain introductions of ICOT activities, and technical papers to more than 600 locations in 35 countries.

We have periodically published and sent more than 1800 technical papers to around 30 overseas locations. We have sent TRs (Technical Reports) and TMs (Technical Memos) on request to foreign addresses. These technical papers consist of more than 700 TRs and 1100 TMs published since the beginning of this project up to January 1992. A third of these technical papers are written in English.

② In the second program ICOT researchers discuss research matters and exchange information with outside researchers.

- ICOT researchers have made more than 450 presentations at international conferences and workshops, and at around 1800 domestic conferences and workshops. They have visited many foreign research organizations to discuss specific research themes and to explain ICOT activities.
- Every year, we have welcomed around 150 to 300 foreign researchers and specialists in other fields to exchange information with them and explain ICOT activities to them.
- As already described in the previous chapter, we have so far invited 74 active researchers from specific technical fields related to FGCS technologies. We have also received six long-term visiting researchers dispatched from foreign governmental organization based on agreement. These visiting researchers conducted research at ICOT and published the results of that research.

③ We sponsored the following symposiums and workshops to disseminate and exchange information on the R&D results and on ICOT activities.

- We hosted the International Conference on FGCS'84 in November 1984. Around 1,100 persons participated and the R&D results of the initial stage were presented. This followed the International Conference on FGCS'81, in which the FGCS project plan was presented. We also hosted the International Conference on FGCS'88 in November 1988. 1,600 persons participated in this symposium, and we presented the R&D results of the intermediate stage.
- We have held
  7 Japan-Sweden (or Japan-Sweden-Italy) workshops since 1983 (co-sponsored with institute or universities in Sweden and Italy),
  4 Japan-France AI symposiums since 1986, (co-sponsored with INRIA of France),
  4 Japan-U.S. AI symposiums since 1987 (co-sponsored with NSF of U.S.A.), and
  2 Japan-U.K. workshops since 1989 (co-sponsored with DTI of U.K.).

Participating researchers have become to known each other well through presentations and discussions during these symposiums and workshops.

- We have also hosted domestic symposiums on this project and logic programming conferences every year.

④ Because the entire R&D cost of this project has been provided by the government, such intellectual property rights (IPR) as patents, which are produced in this project, belong to the Japanese government. These IPR are managed by AIST (Agency of Industrial Science and Technology). Any company wishing to produce commercial products that use any of these IPR must get permission to use them from AIST. For example, PSI and SIMPOS have already been commercialized by companies licensed by AIST. The framework for managing IPR must impartially utilize IPR acquired through this project. That is, impartial permission to domestic and foreign companies, and among participating companies or others is possible because of AIST.

⑤ Software tools developed in this project that are not yet managed as IPR by AIST can be used by other organizations for non-commercial aims. These software tools are distributed by ICOT according to the research tools permission procedure. We, now, have more than 20 software tools, such as PIMOS, PDSS, Kappa-II, the A'um system, LTB, the CAP system, the cu-prolog system and the TRS generator.
In other cases, we make the source codes of some programs public by printing them in technical papers.

⑥ On specific research themes in the logic programming field, we have collaborated with organizations such as Argonne National Laboratory (ANL), National Institute of Health (NIH), Lawrence Berkeley Laboratory (LBL), Swedish Institute of Computer Science (SICS) and Australia National University (ANU).

5 Forecast of Some Aspects of 5G Machines

LSI technologies have advance in accordance with past trends. Roughly speaking, the memory capacity and the number of gates of a single chip quadruple every three years. The number of boards for the CPU of an inference machine was more than ten for PSI- I , but only three for PSI- II and single board for PIM.

The number of boards for 80M bytes memory was 16 for PSI- I , but only four for PSI- II and a single for PIM (m).

Figure 5-1 shows the anticipated trend in board numbers for one PE (processor element: CPU and memory) and cost for one PE based on the actual value of inference machines developed by this project.

The trend shows that, by the year 2000, around ten PEs will fit on one board, around 100 PEs will fit in one desk side cabinet, and 500 to a 1,000 PEs will fit in a large cabinet. This trend also shows that the cost of one PE will halve every three years.

Figure 5-2 shows the performance trends of 5G machines based on the actual performance of inference machines developed by this project.

The sequential inference processing performance for one PE quadrupled every three years. The improvement in parallel inference processing performance for one PE was not as large as it was for sequential processing, because PIM performance is estimated at around two and one half times that

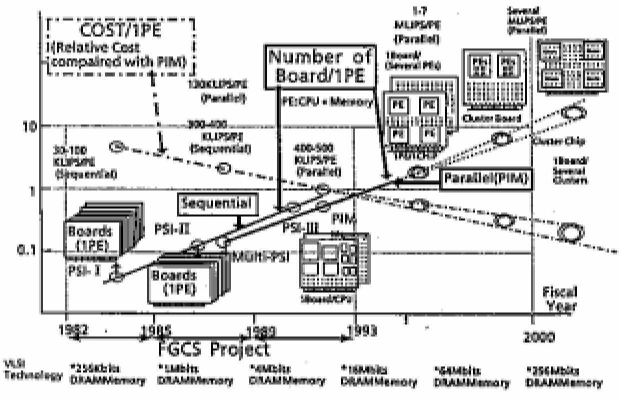

Figure 5-1 Size and cost trends of 5G machines

of multi-PSI. Furthermore, Figure 5-2 shows the performance of one board for both sequential and parallel processing, and the performance of a conventional micro-processor with CISC and RISC technology. In this figure, future improvements in the performance of one PE are estimated to be rather lower than a linear extension of past values would indicate because of the uncertainty of whether future technology will be able to elicit such performance improvements. Performance for one board is estimated at about 20 MLIPS, which is 100 times faster than PIM. Thus, a parallel machine with a large cabinet size could have 1 GLIPS. These parallel systems will have the processing speeds needed for various knowledge processing applications in the near future.

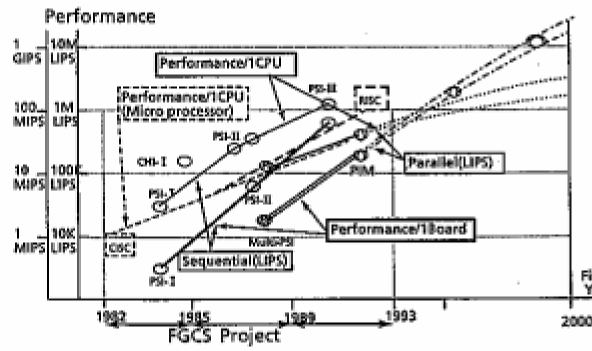

Figure 5-2 Performance trends of 5G machines

Several parallel applications in this project, such as CAD, theorem provers, genetic information processing, natural language processing, and legal reasoning are described in Chapter 2. These applications are distributed in various fields and aim at cultivating new parallel processing application fields.

We believe that parallel machine applications will be extended to various areas in industry and society, because parallel technology will become common for computers in the near future. Parallel application fields will expand gradually according to function expansion by the use of advanced parallel processing and knowledge processing technologies.

6 Final Remarks

I believe that we have shown the basic framework of the fifth generation computer based on logic programming to be more than mere hypothesis. By the end of the initial stage, we had shown the fifth generation computer to be viable and efficient through the development of PSI, SIMPOS and various experimental software systems written in ESP and Prolog.

I believe that by the end of the intermediate stage, we had shown the possibility of realizing the fifth generation computer through the development of a parallel logic programming software environment which consisted of multi-PSI and PIMOS.

And I hope you can see the possibility of an era of parallel processing arriving in the near future by looking at the prototype system and the R&D results of the FGCS Project.

Acknowledgment

This project has been carried out through the efforts of the researchers at ICOT, and with the support of MITI and many others outside of ICOT. We wish to extend our appreciation to them all for the direct and indirect assistance and co-operation they have provided.

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